2.5 W AMPLIFIER FOR 11 GHz 1800 FDM CHANNELS SYSTEM

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Abstract

This paper describes the design and development of an 11 GHz amplifier, suitable for FDM signals and using a divider-amplifier-multiplier chain. The overall power amplifier in the 10.7-11.7 GHz bandwidth provides a 32 dB gain, a typical 5.7% efficiency and a 2.5 W power output with expected reliability exceeding 200,000 hours.
This amplifier not only has better performances than the well-known Impatt solution, but it is also competitive with FET amplifiers now available on the market.

Introduction

In designing the divider-amplifier-multiplier chain (Ref.1) the best technical and economical solution is a compromise between the following factors:
- division and multiplication order
- power and amplification capability of the transistors
- mechanical complexity
- total cost

A list of possible solutions to be considered to fulfill the best compromise is given in table 1.

At present solution 1 and 2 are not feasible, since no commercial solid-state, bipolar or Mesfet, device gives a sufficient output power.
However, by paralleling two or more devices it is possible to obtain the necessary output power, but the total efficiency becomes very poor, while the mechanical complexity and total costs considerably increase.
On the contrary, high values of n will result in:
- higher input levels required by the frequency divider to perform the proper locking bandwidth with an acceptable noise contribution;
- higher losses of the multiplier with consequent difficulty to ensure the proper junction temperature required for a good reliability.

The solution adopted has:
- a division and multiplication order by 4 with a bipolar amplifier operating in the 2.65 to 2.950 GHz bandwidth;
- the final section of the amplifier realized with two paralleled amplifier-multiplier chains.

Figure 1 shows the block diagram of the overall amplifier with minimum values of the levels.

Table 1

Solut. N°	Multipl. Divis. order n	Amplif.Freq. (MHz)	Total Multipl. losses (dB)	Ampl.output power (dBm)	Overall output power (dBm)
1	2	5.350-5.850	3	+37	+34
2	3	3.560-3.900	4.5	+38.5	+34
3	4	2.650-2.950	6	+40	+34
4	5	2.140-2.340	7.5	+41.5	+34

Possible solutions of the 11 GHz divider-amplifier-multiplier chain

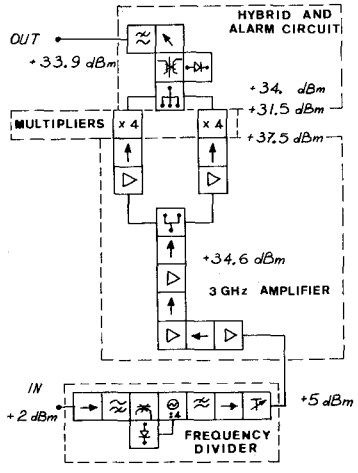

Fig.1 Block diagram of the overall amplifier

Power splitting at 3 GHz and power combining at 11 GHz are performed by microstrip 3 dB rat race hybrids.
This solution allows to obtain:
- best system availability;
- final transistors and varactor diodes operate in better thermal conditions than the ones obtainable with only one final transistor and varactor diode multiplier.

The two signals are easily and exactly phase added, trimming the phase shifting networks located in the input networks of the final amplifiers and measuring the unbalancing of the output hybrid dummy port.
When lower output power is required the mechanical structure adopted easily allows to realize a single final chain version performing a 1.5 W output power with further optimization of reliability and cost.
Both 3 and 11 GHz circuits have been developed on microstrips deposited on a teflon-fiberglass.

Design and development

The complete amplifier can be divided in four fundamental parts: divider, amplifier, multiplier and output hybrid with alarm circuit.
The frequency divider and 3 GHz amplifier are located in one single flat aluminum box, connected to the dissipating front panel and supporting the multipliers and output hybrid box.

Frequency divider

Frequency division-by-four is performed with a harmonic injection-locked 3 GHz oscillator. This oscillator has been studied by Adler and Kurokawa (2), (3). Further papers have stated the good performance of the injection-locked oscillator frequency divider with FM signals (4), (5).
The main conditions to optimize the gain bandwidth of the injection-locked frequency divider are as follows:
- a high cut-off frequency of the oscillator transistor;
- a proper bias point to increase the non-linearity of the transistor.

The injection signal at 11 GHz is applied to the base of the oscillator transistor through a teflon microstrip isolator and a WR75 waveguide trunk acting as a high-pass filter.
The isolator insertion loss is less than .5 dB.
A temperature sensitive loop keeps the transistor temperature constant, when the ambient temperature ranges from 0° to 45°C.
In this way, the ambient temperature does not affect the free frequency oscillator within $\pm$ 5 MHz and the injection locked bandwidth.
The power level obtainable at the divider output is roughly +6 to 9 dBm, depending upon the bias point. However, a proper variable attenuator allows to adjust the output level to +5 dBm.
The minimum locking bandwidth at 11 GHz is greater than 200 MHz.
Four sub-ranges are needed to completely cover the 10.7 to 11.7 GHz bandwidth. In each sub-range the divider can be easily tuned by simply acting on the oscillator tuning screw.
A directional coupler, detector and alarm circuit turn off the oscillator, should the 11 GHz signal not be present.

3 GHz amplifier

As is shown in fig. 1, the complete 3 GHz amplifier is formed by two class A amplifier stages followed by two stages using matched transistors driving the final power device parallel through a 3 dB hybrid. Each way gives a 5.5 W power.
The input and output matching networks of each class A amplifier stage have been designed by using scattering parameters, obtained from a set of measurements at the Automatic Network Analyzer. (6)
Then by using a "Compact" computer program, the circuit has been optimized in order to achieve a flat gain over the bandwidth, a good VSWR and stability.
The thick film bias networks are placed on the same teflon-fiberglass board where the input and output matching networks are arranged.

The devices in the class C amplifier stages are internally matched to 50 ohm, at the input as well as at the output.
The main features of the final stages are:

- input power 31 dBm
- output power 37.5 dBm
- V_{CB} 24 V
- I_{CB} 550 mA
- Thermal resistance 8°C/W

The operating conditions of the final transistor prevents its junction temperature from reaching 140°C at the maximum ambient temperature of 45°C.

All amplifier transistors must be adequately selected and tested in accordance with the supplier.
This in order to guarantee the RF performance and ensure the previously mentioned MTTF.
Incoming acceptance of low-level transistors are made with an Automatic Network Analyzer on the basis the MAGs (or MSG if K is less than 1) measured at the maximum working frequency.
For high-level transistors selection is carried out with proper RF text fixture.(Fig. 2)

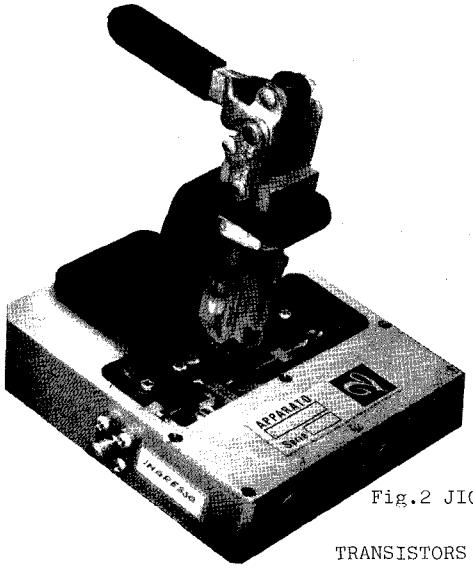

Fig.2 JIG FOR MICROWAVE TRANSISTORS TESTING

Multiplier

The multiplier is composed of:

- an input matching network;
- a diode;
- an output filter.

The input matching network is made up of semi-lumped π capacitors mounted on a teflon-fiberglass substrate. A return loss greater than 20 dB over a bandwidth of approx. 75 MHz at 3 GHz can be obtained.

Also the resistor for the self-biasing diode is placed in the sub-strate.
The output filter is realized by three coaxial resonators, the first one of which is directly coupled to the diode.
The total multiplier losses are less than 6 dB over an instantaneous bandwidth of 300 MHz at 11 GHz.
The 3rd and 5th harmonics are at least 60 dB down.
The maximum junction temperature of the three-junction diode is less than 120°C at the maximum heat sink temperature of 65°C. The multiplier is shown in fig. 3.

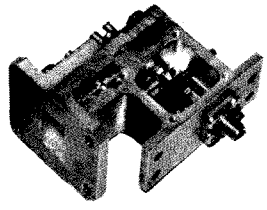

Fig. 3 Multiplier-by-four

3 dB Hybrid and Alarm circuit

The multiplier outputs feed a rat race hybrid by two adaptors from the WR75 waveguide to the microstrip.
By means of the same adaptors the hybrid output energizes a WR75 waveguide trunk, where two directional coupler waveguide microstrips are placed (7).
The first one feeds a monitoring output, while the second one feeds a detector diode driving the alarm circuit.
The total loss is less than .8 dB.

Performance

The complete amplifier has a nominal gain of 32 dB with a 2.5 W output power.
It is driven by +24 Vdc power supply at 2 A maximum.
Typical and minimum values of the overall efficiency are 5.7% and 5.4%, respectively.
Figure 4 shows the AM to PM conversion measured with a dynamic method at an 8 MHz BB modulating frequency.

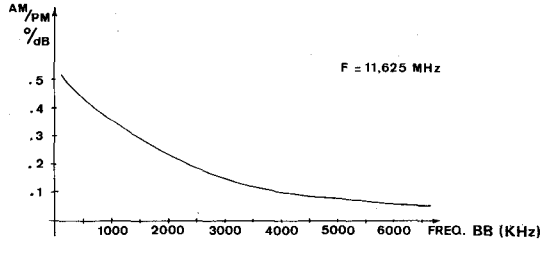

Fig. 4 Behaviour of AM/PM conversion

The FM noise of the divider is less than 5 pWOp in the 7.6 MHz baseband slot and the intermodulation noise of the amplifier is less than 2 pWOp.
In the ambient temperature range of 0 to 45°C the maximum variation of the output power is .8 dB.
When the amplifier module is mounted in the radio link rack the maximum internal overtemperature is 20°C, with respect to the ambient temperature.
The pictures of fig. 5 and fig. 6 show the complete amplifier and the output hybrid, respectively.

Conclusions

A complete divider-amplifier-multiplier chain operating in the 10.7 to 11.7 GHz band with a 2.5 W output power, a 32 dB gain and a 5.4% minimum efficiency has been described.
The amplifier is particularly optimized as far as reliability and cost are concerned.
The 2.5 W amplifier has been adopted in an 11 GHz 1800 channels equipment for a short-haul radio link.
The same equipment will be used in Italy for a cross band diversity system in conjunction with a 7 GHz radio link.

Acknowledgements

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References

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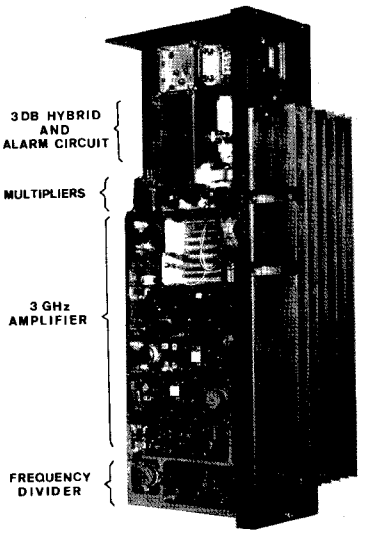

Fig. 5 Solid-state amplifier

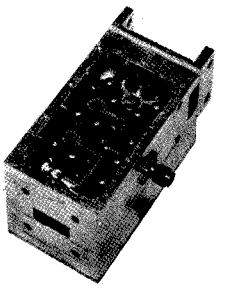

Fig. 6 3 dB hybrid and alarm circuits